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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yasuhisa SHIMAZAKI et al.

Appln. No.: 09/855,660 Group Art Unit: 2819

Filed: May 16, 2001 Examiner: D. Chang

For: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING HIGH-SPEED AND LOW-POWER LOGIC GATES WITH COMMON TRANSISTOR SUBSTRATE POTENTIALS, AND DESIGN DATA RECORDING

MEDIUM THEREFOR

THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any assertion as to materiality or prior art effect, the documents listed on the attached Form PTO-1449 are hereby cited.

The listed Japanese documents were cited in a recent

Office Action regarding a counterpart Japanese application.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

Mitchell W. Shapiro

Reg. No. 31,568

MWS:lat

Miles & Stockbridge P.C. 1751 Pinnacle Drive Suite 500 McLean, Virginia 22102-3833 (703) 610-8652

February 23, 2004

FORM PTO-1449					Atty. Docket No.			Appln. No.	
LIST OF DOCUMENTS CITED BY APPLICANT					XA-9472			09/855,660	
PE					Applicant				
					Yasuhisa SHIMAZAKI et al.				
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	AL	11-224901	8/17/99	Japan					Abstract
	AM	05-299624	11/12/93	Japan					Abstract
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conformance and not considered. Include copy of this form with next communication to Applicant.